multiLane

DATASHEET

Innovation for the next generation

ML4079E(N)

8 Channel | 56 GBd PAM4 & NRZ | 800G BERT

8 x 56 GBd NRZ/PAM4 BERT | SSPRQ, PRBS13Q & PRBS31Q | TX and RX Equalizers | Real FEC analysis| Crosstalk noise injection

Summary

With the accelerated growth of hyperscale datacenters, the performance demands on Ethernet network infrastructure is increasing exponentially, and customer expectations for high-speed data throughput is at an all-time high. As a result, Bit Error Rate Testers (BERT) have become the cornerstone for physical layer testing, from testing fiber optic and copper wire digital data transmission lines to testing signal integrity of transceivers.

The ML4079E is an 800G BERT ready to support the newly emerging 8 x 100 Gbps technology cycle. Most importantly it supports real hardware FEC analysis to be able to understand the DUT behavior in a system environment. Other features include signal-to-noise ratio (SNR) and histogram measurements, as well as transmitter and receiver equalizers.

In addition, receiver stress and jitter tolerance testing can be supported by this platform. ML4079EN supports direct crosstalk and noise injection, and both ML4079E as well as ML4079EN can be combined with the ML407-PAM jitter clock source for jitter tolerance testing.

ML4079E

8 x 56 GBd PAM4 BERT

Introduction

The ML4079E is a full featured 800G BERT that can be configured as eight channels of 23-29 and 46-58 GBaud PAM4 or 23-29 and 46-58 Gbps NRZ.

The transmitters support all standard test patterns mandated by IEEE and OIF such as PRBS13Q, SSPRQ, PRBS31Q, etc. Additionally, the user may program the TX to output a user-defined pattern up to 131 kb long.

In addition, the ML4079E supports transmitter and receiver equalization to overcome signal integrity impairments due to channel losses or reflections.

Key Features

Transmit

- Data Rates: 23-29 & 46-58 GBaud (116 Gbps)
- Ability to tune the bit rate in steps of 100 kbps and find the RX PLL locking margin.
- Independent control of inner eye levels
- Up to 1.5 Vppd output swing
- Supports Gray coding and polarity inversion
- Error injection
- 3-tap LUT-based Pre- and Post-emphasis or 7-tap linear FFE

Available patterns are:

- PRBS 7/9/11/13/15/16/23/31/58 and their inverses
- PRBS13Q, PRBS31Q
- SSPRQ
- Square wave

Receive

- Programmable front-end attenuator
- SNR monitoring over time.
- PAM histogram monitor.
- PAM slicer threshold adjustable.
- Error-detection on following patterns:
  - PRBS 7/9/11/15/16/23/31
  - PRBS13Q and PRBS31Q
- Automatic pattern detects
- LOS indicators.

General

- LabView driver and Python wrapper available.
- API libraries with documentation.

Target Applications

- Testing of copper and fiber-optic transmission lines
- Functional and SI testing of transceivers

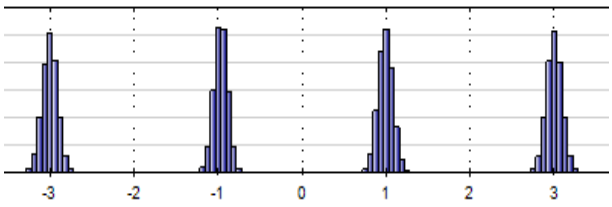

Figure 1: PAM eye histogram

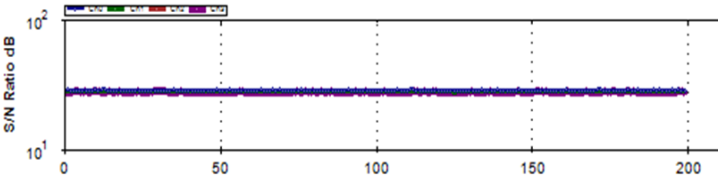

Figure 2: S/N Ratio over 200 captures

Crosstalk

Integrated Crosstalk Noise, available on a per lane basis, and programmable in increments of 0.5 mV. Available on ML4079EN only.

FEC - Important feature

Supports real hardware FEC. Pre- and post-FEC BER/SER, and FEC margin available on channels individually as well as on 100G, 400G, 800G blocks.

Specifications*

Parameter	Specifications
Bit Rates	23 – 29 GBaud / 46 – 58 GBaud
TX Amplitude Differential	0 – 700 mVpp
Patterns	PRBS13Q, 31Q and SSPRQ Square wave
TX Amplitude Adjustment	Steps of 1 mV
Pre-emphasis resolution	1000 steps
Pre- / Post-emphasis	6 dB
Equalizing Filter Spacing	1 UI
Random Jitter RMS	< 290 fs[1]
Rise/ Fall Time (20–80%) [1]	< 10 ps
Coding	Gray coding supported
Output Return Loss up to 10GHz	< -15 dB
Output Return Loss (16-25GHz)	< -10 dB
Error Detector input range	50 – 800 mV diff.
TX/RX connectors	Core HC2, 2.5 mm 8 channel foot print
Reference clock Output	Rate division 4/8/16/32/128/256
Diff. Input Return Loss	Better than 10 dB
Eye monitor resolution	8 bits horizontal across 2 UI / 9 bits vertical
Clock Input Range	Up to 4.4 GHz
Clock Input Amplitude	200 - 1000 mV
Input Impedance	50 Ω
Temperature range	0-75 °C
Power	110 V, 1.4 A or 220 V, 0.9 A – 50/60 Hz
Power (ATE version only)	12 V, 1.5 A

* Specifications are subject to change.

[1] With appropriate pre and post emphasis settings and 50 GHz scope. Trigger from adjacent data channel rate/8

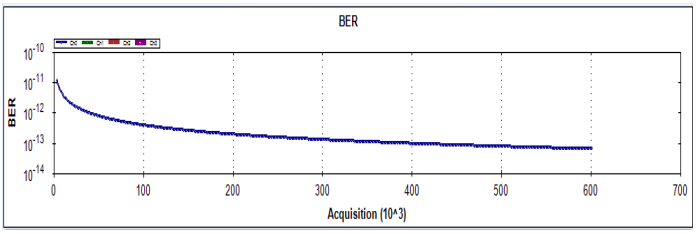

Figure 3: BER curves for one channel with 1 error inserted at the MSB and LSB respectively

Mechanical Dimensions

Ordering Information

Option	Description
ML4079E	800G BERT (8 CH 56 GBd PAM4)
ML4079EN	800G BERT (8 CH 56 GBd PAM4) with crosstalk noise injection
3YW	Total 3-year warranty
CAL	Single calibration
3YWC	Total 3-year warranty with 3 annual calibrations
FEC	Real Hardware FEC analysis

Recommended Accessories

Instruments	Recommended *Phase matched cable pairs*	Comments
ML4079E	4x TM40-0334-01	4x Core HC2, 2.5 mm 8 ch to 2.4 mm male connector, 10 inch length
ML4079EN	4x TM40-0334-01	4x Core HC2, 2.5 mm 8 ch to 2.4 mm male connector, 10 inch length

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