ML4057/ML4057-ACO

MSA Compliant

CFP8/CFP8-ACO MCB

Rev 0.1

multiLane

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1. General Description

ML4057 is designed to provide an easy and effective solution for programming and characterization of CFP8 modules. The ML4057 comes complete with a user friendly GUI supporting all features defined by CFP8 MSA and simplifying configuration process. Current sense circuit is also included on the Host, for checking modules power class.

2. ML4027-ACO CFP2-ACO test board - Key Features

- ✓ Supports 16x25G, 8x50G PAM and CFP8-ACO
- ✓ MDIO MSA compliant master
- ✓ 2x8 40GHz Huber & Suhner _2x8A_81_MXP-S50-0-3-111_N Connectors
- ✓ Module Current Sense
- ✓ Low Insertion Loss using RO4350 PCB materials
- ✓ Matched length differential pairs 2147 mils
- ✓ High performance signal integrity traces from Connectors to interface
- ✓ On-board LEDs showing MSA output Alarms states
- ✓ On-board buttons/jumpers for MSA input control signals
- ✓ User friendly GUI for MDIO control and loading custom MSA Memory Maps
- ✓ USB controlled

3. Operating Conditions

Recommended Operation Conditions						
Parameter	**Symbol**	**Notes/Conditions**	**Min**	**Typ**	**Max**	**Units**
Operating Temperature	T_A		0		85	°C
Supply Voltage	VCC	Main Supply Voltage (from external PS)	3.00	3.3	3.60	V
Supply Voltage	VCC	Supply voltage from DC adapter		5		V

3.1. LEDs

The LED D11 indicates whether a USB cable is plugged or not.
The other two LEDs, D12 and D13, are used for diagnostic purposes.

- If the green LED, D13, is on: USB is locked and device is recognized by the USB driver.
- If the red LED, D12, is on: USB not connected or USB driver not found.
- If both LEDs are off: Board not powered correctly or firmware is corrupted.

4. Power Supplies

The board can be powered using a 3.3V external power supply through banana plugs U6, U7, or using a 5V DC adapter jack with J2.

A current sense is available on the board, and it measures the current draw on the main P3V3 net.

5. CFP2 HW Signaling Pins

Hardware alarm pins, hardware control pins and MDIO pins can be accessed from the software via USB or through on-board LEDs and pin headers. The lower part of dip switch U153 (**1**) allows switching signaling pins control between software and hardware (switch to side where it's indicated ***ON*** for hardware control). And the upper part of U153 (**2**) allows to operate the board via external MDIO (switch to side where it's indicated ***ON*** for external MDIO control).

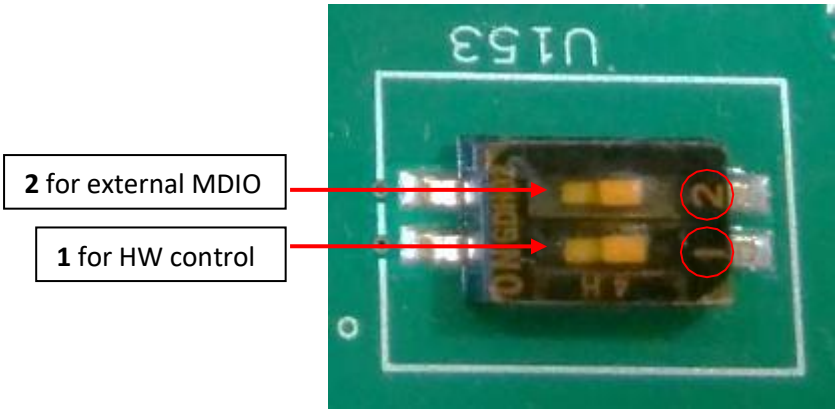


Figure 1: Dip switch U153

All Hardware Alarm signals can be accessed through test points or LEDs shown below:

Figure 2: HW alarm signals

All hardware control signals can be driven through the jumpers shown below:

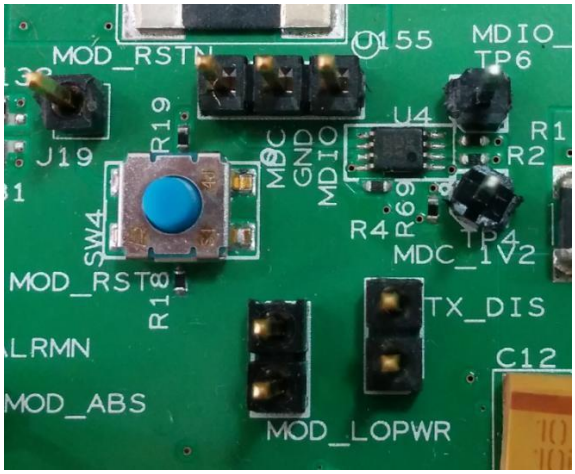


Figure 3: HW control signals jumpers

Below are the pin headers for the MDIO interface:

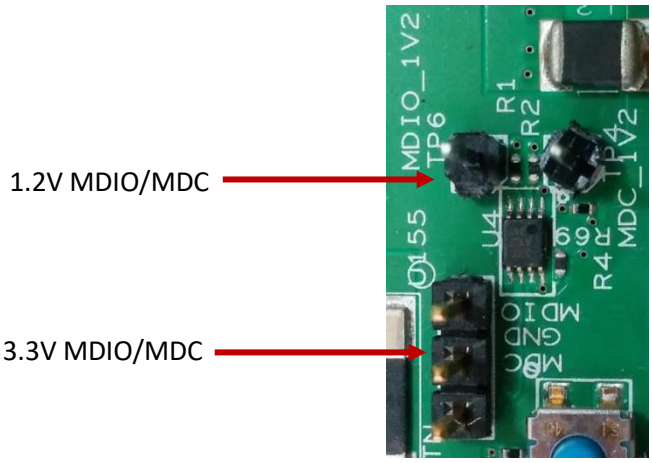
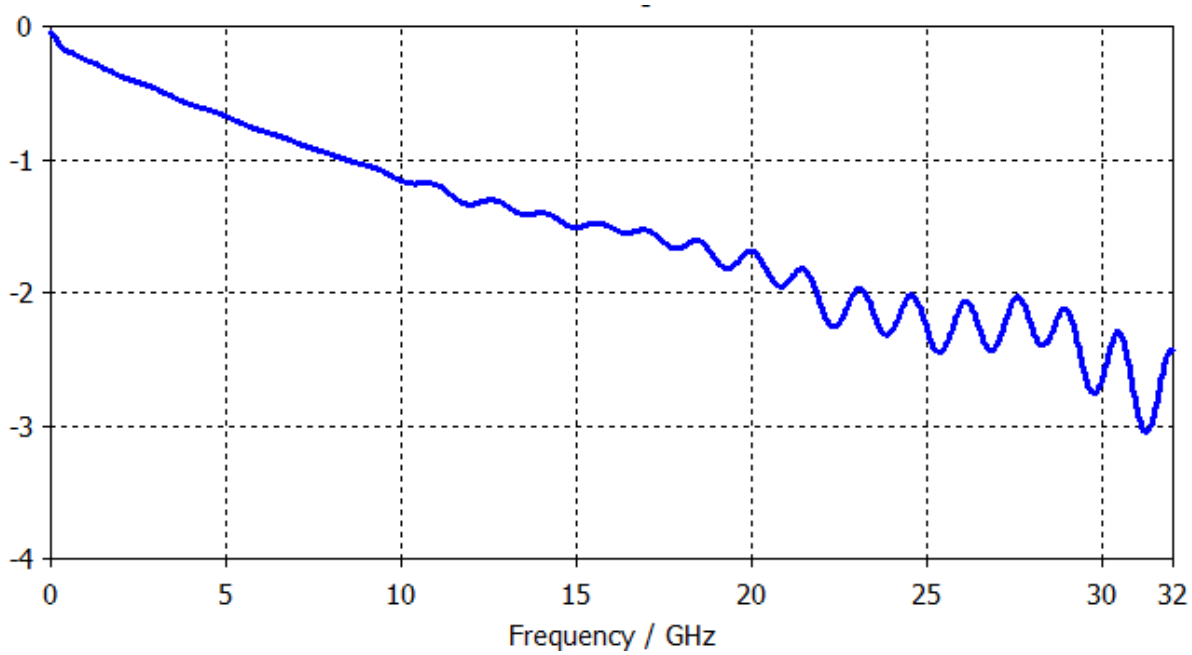


Figure 4: MDIO pin headers

6. High Speed Signals

6.1.1. S-Parameters

All TX and RX channels on the board have the same trace length and geometry. A differential test trace of same length and geometry as the channels is available on the board to be used for de-embedding the MCB traces from the measurements.



6.2. Reference Clock

REFCLK N/P, TX_MCLK N/P and RX_MCLK N/P are accessible through SMP connectors and are AC coupled.

7. CFP8/CFP8-ACO Graphical User Interface

This GUI supports CFP8 and CFP8-ACO boards. To switch between the two, the ACO checkbox is used (figure below). Check it for ACO mode.

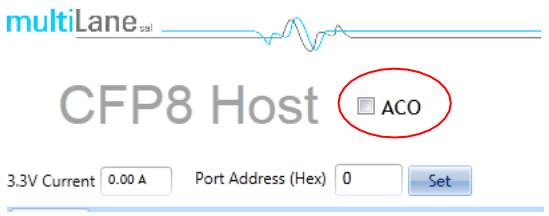


Figure 5: ACO mode

7.1. Communication Window

This is the main interface used for initial communication with the host.

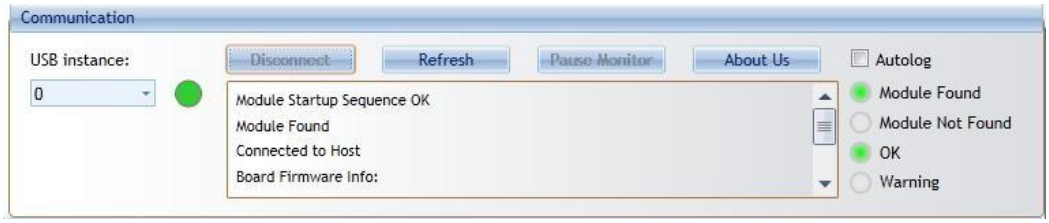


Figure 6: Communication Window

The Initialize button is the application's main entry point, used to establish a connection with the CFP8 Host board and the Module. Once a USB connection is established, the Host checks if a CFP8 Module is inserted, and accordingly illuminates the corresponding (*Module Found* or *Module Not Found*) LED. And when the USB connection is lost, the *USB Error* LED is illuminated.

The status box window in the GUI will show any success or failure messages that are being returned as a result of the GUI communicating or attempting to communicate with the hardware.

- *Refresh* button: checks for connection status, refresh Hardware Readings and updates GUI.
- *Pause Monitor* button: Pause/Resume monitoring.
- *About Us* button: shows program information (name, version) and company information.

Note that multiple boards can be connected via USB. The desired board is selected using *USB Instance* field from the *Communication* window.

7.2. Monitor tab

The Monitor tab is the main source of the module status and alarm/warning flags conditions. It shows the current status of a flag, the default flag update rate is 2 Hz, so the flag status is updated every 0.5 seconds.

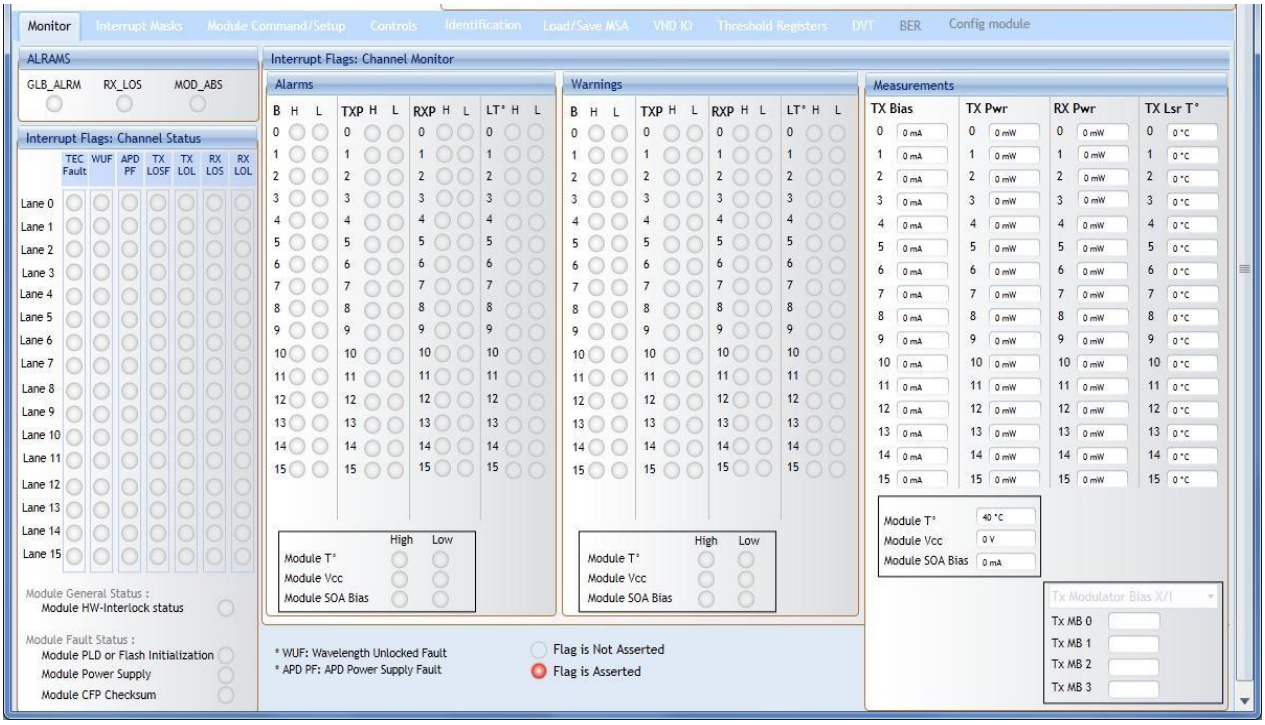


Figure 7: Monitor tab

7.2.1. Flag Statuses:

- Flag is not asserted: the corresponding LED is OFF (Transparent).
- Flag is asserted: the corresponding LED is ON (Red).

7.2.2. Corresponding MSA registers for channel monitor

ACO mode:

B180 [2.0]	**16**	**RO**		**Network Lane n Alarm and Warning 1**	**16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent.**	**0000h**
			15	Bias High Alarm	0: Normal; 1: Asserted. (FAWS_TYPE_C)	0
			14	Bias High Warning	0: Normal; 1: Asserted. (FAWS_TYPE_C)	0
			13	Bias Low Warning	0: Normal; 1: Asserted. (FAWS_TYPE_C)	0
			12	Bias Low Alarm	0: Normal; 1: Asserted. (FAWS_TYPE_C)	0
			11	TX Power High Alarm	0: Normal; 1: Asserted. (FAWS_TYPE_C)	0
			10	TX Power High Warning	0: Normal; 1: Asserted. (FAWS_TYPE_C)	0
			9	TX Power Low Warning	0: Normal; 1: Asserted. (FAWS_TYPE_C)	0
			8	TX Power Low Alarm	0: Normal; 1: Asserted. (FAWS_TYPE_C)	0
			7	Laser Temperature High Alarm	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0
			6	Laser Temperature High Warning	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0
			5	Laser Temperature Low Warning	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0
			4	Laser Temperature Low Alarm	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0
			3	RX Power High Alarm	0: Normal; 1: Asserted. (FAWS_TYPE_B) The thresholds for the RX Power High/Low Alarm/Warning are determined by the RX Power Monitor Alarm/Warning Threshold Select in B015h. This comment applies to bits 2~0 as well.	0
			2	RX Power High Warning	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0
			1	RX Power Low Warning	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0
			0	RX Power Low Alarm	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0

Figure 8: Interrupt flags alarms and warnings (ACO)

Normal mode:

A200	**16**	**RO**		**Network Lane n Alarm and Warning**	**16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent.**	**0000h**
			15	Bias High Alarm	0: Normal; 1: Asserted. (FAWS_TYPE_C)	0
			14	Bias High Warning	0: Normal; 1: Asserted. (FAWS_TYPE_C)	0
			13	Bias Low Warning	0: Normal; 1: Asserted. (FAWS_TYPE_C)	0
			12	Bias Low Alarm	0: Normal; 1: Asserted. (FAWS_TYPE_C)	0
			11	TX Power High Alarm	0: Normal; 1: Asserted. (FAWS_TYPE_C)	0
			10	TX Power High Warning	0: Normal; 1: Asserted. (FAWS_TYPE_C)	0
			9	TX Power Low Warning	0: Normal; 1: Asserted. (FAWS_TYPE_C)	0
			8	TX Power Low Alarm	0: Normal; 1: Asserted. (FAWS_TYPE_C)	0
			7	Laser Temperature High Alarm	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0
			6	Laser Temperature High Warning	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0
			5	Laser Temperature Low Warning	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0
			4	Laser Temperature Low Alarm	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0
			3	RX Power High Alarm	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0
			2	RX Power High Warning	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0
			1	RX Power Low Warning	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0
			0	RX Power Low Alarm	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0

Figure 9: Interrupt flags alarms and warnings

7.2.3. Corresponding MSA registers for channel status

ACO mode:

B1A0 [2.0]	**16**	**RO**		**Network Lane n Fault and Status**	**16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent.**	**0000h**
			15	Lane TEC Fault	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0
			14	Lane Wavelength Unlocked Fault	0: Normal; 1: Asserted. (FAWS_TYPE_C)	0
			13	Lane APD Power Supply Fault	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0
			12~8	Reserved		0
			7	Lane TX_LOSF	0: Normal; 1: Asserted. (PMD) (FAWS_TYPE_C)	0
			6	Lane TX_LOL	0: Normal; 1: Asserted. (Network) (FAWS_TYPE_B)	0
			5	Reserved		0
			4	Lane RX_LOS	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0
			3	Lane RX_LOL	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0
			2	Lane RX FIFO error	0: Normal, 1: Error. (FAWS_TYPE_B)	0
			1	Lane RX TEC Fault	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0
			0	Reserved.		0

Figure 10: Channel status registers (ACO)

Normal mode:

A210	**16**	**RO**		**Network Lane n Fault and Status**	**16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent.**	**0000h**
			15	Lane TEC Fault	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0
			14	Lane Wavelength Unlocked Fault	0: Normal; 1: Asserted. (FAWS_TYPE_C)	0
			13	Lane APD Power Supply Fault	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0
			12~8	Reserved		0
			7	Lane TX_LOSF	0: Normal; 1: Asserted. (PMD) (FAWS_TYPE_C)	0
			6	Lane TX_LOL	0: Normal; 1: Asserted. (Network) (FAWS_TYPE_B)	0
			5	Reserved		0
			4	Lane RX_LOS	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0
			3	Lane RX_LOL	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0
			2	Lane RX FIFO error	0: Normal, 1: Error. (FAWS_TYPE_B)	0
			1	Reserved.		0
			0	Reserved.		0

Figure 11: Channel status registers

7.2.4. Corresponding MSA registers for module alarm and warning

ACO mode:

B01F [2.0]	1	RO		Module Alarm and Warning 1		0000h
			15~12	Reserved		0000b
			11	Mod Temp High Alarm	Mod temp high Alarm. (FAWS_TYPE_A) 0: Normal, 1: Asserted.	0
			10	Mod Temp High Warning	Mod temp high Warning. (FAWS_TYPE_A) 0: Normal, 1: Asserted.	0
			9	Mod Temp Low Warning	Mod temp low Warning. (FAWS_TYPE_A) 0: Normal, 1: Asserted.	0
			8	Mod Temp Low Alarm	Mod temp low Alarm. (FAWS_TYPE_A) 0: Normal, 1: Asserted.	0
			7	Mod Vcc High Alarm	Input Vcc high Alarm. (FAWS_TYPE_A) 0: Normal, 1: Asserted.	0
			6	Mod Vcc High Warning	Input Vcc high Warning. (FAWS_TYPE_A) 0: Normal, 1: Asserted.	0
			5	Mod Vcc Low Warning	Input Vcc low Warning. (FAWS_TYPE_A) 0: Normal, 1: Asserted.	0
			4	Mod Vcc Low Alarm	Input Vcc low Alarm. (FAWS_TYPE_A) 0: Normal, 1: Asserted.	0
			3	Mod SOA Bias High Alarm	SOA bias current high alarm. (FAWS_TYPE_B)	0
					0: Normal, 1: Asserted.	
			2	Mod SOA Bias High Warning	SOA bias current high warning. (FAWS_TYPE_B) 0: Normal, 1: Asserted.	0
			1	Mod SOA Bias Low Warning	SOA bias current low warning. (FAWS_TYPE_B) 0: Normal, 1: Asserted.	0
			0	Mod SOA Bias Low Alarm	SOA bias current low alarm. (FAWS_TYPE_B) 0: Normal, 1: Asserted.	0

Figure 12: Module alarm and warning (ACO)

Normal mode:

B01F [2.0]	1	RO		Module Alarm and Warning 1		0000h
			15~12	Reserved		0000b
			11	Mod Temp High Alarm	Mod temp high Alarm. (FAWS_TYPE_A) 0: Normal, 1: Asserted.	0
			10	Mod Temp High Warning	Mod temp high Warning. (FAWS_TYPE_A) 0: Normal, 1: Asserted.	0
			9	Mod Temp Low Warning	Mod temp low Warning. (FAWS_TYPE_A) 0: Normal, 1: Asserted.	0
			8	Mod Temp Low Alarm	Mod temp low Alarm. (FAWS_TYPE_A) 0: Normal, 1: Asserted.	0
			7	Mod Vcc High Alarm	Input Vcc high Alarm. (FAWS_TYPE_A) 0: Normal, 1: Asserted.	0
			6	Mod Vcc High Warning	Input Vcc high Warning. (FAWS_TYPE_A) 0: Normal, 1: Asserted.	0
			5	Mod Vcc Low Warning	Input Vcc low Warning. (FAWS_TYPE_A) 0: Normal, 1: Asserted.	0
			4	Mod Vcc Low Alarm	Input Vcc low Alarm. (FAWS_TYPE_A) 0: Normal, 1: Asserted.	0
			3	Mod SOA Bias High Alarm	SOA bias current high alarm. (FAWS_TYPE_B)	0
					0: Normal, 1: Asserted.	
			2	Mod SOA Bias High Warning	SOA bias current high warning. (FAWS_TYPE_B) 0: Normal, 1: Asserted.	0
			1	Mod SOA Bias Low Warning	SOA bias current low warning. (FAWS_TYPE_B) 0: Normal, 1: Asserted.	0
			0	Mod SOA Bias Low Alarm	SOA bias current low alarm. (FAWS_TYPE_B) 0: Normal, 1: Asserted.	0

Figure 13: Module alarm and warning

7.2.5. Corresponding MSA registers for module general and fault statuses

ACO mode:

B01D [2.0]	**1**	**RO**		**Module General Status**		**0000h**
			15	Reserved		0
			14	Reserved		0
			13	HW_Interlock	Module internally generated status signal. (FAWS_TYPE_A) 0: If module power <= Host cooling capacity or if hardware Interlock is not used, 1: If module power > Host cooling capacity. For non-pluggable modules (e.g. MSA-100GLH module), PRG_CNTL3 pin should be set to "1" during initialization state.	0

Figure 14: Module general status (ACO)

B01E [2.0]	**1**	**RO**		**Module Fault Status**	**Module Fault Status bit pattern. Only fatal faults that are potentially harmful to the module can trigger the bits here. All the bits are 0: Normal; 1: fault detected. When any bit in this register is a '1', The Module State register will also be set to the Fault State.**	**0000h**
			15	Reserved	Reserved for extension of "other faults" in case of all the bits used up in this register.	0
			14~7	Reserved		0
			6	PLD or Flash Initialization Fault	PLD, CPLD, or FPGA initialization fault. (FAWS_TYPE_A)	0
			5	Power Supply Fault	1: Power supply is out of range. (FAWS_TYPE_A)	0
			4~2	Reserved		000b
			1	CFP Checksum Fault	1: CFP Checksum failed. (FAWS_TYPE_A)	0
			0	Reserved		0

Figure 15: Module fault status (ACO)

Normal mode:

A01D	**1**	**RO**		**Module General Status**		**0000h**
			15	Reserved		0
			14	Reserved		0
			13	HW_Interlock	Module internally generated status signal. (FAWS_TYPE_A) 0: If module power <= Host cooling capacity or if hardware Interlock is not used, 1: If module power > Host cooling capacity.	0

Figure 16: Module general status

A01E	**1**	**RO**		**Module Fault Status**	**Module Fault Status bit pattern. Only fatal faults that are potentially harmful to the module can trigger the bits here. All the bits are 0: Normal; 1: fault detected. When any bit in this register is a '1', The Module State register will also be set to the Fault State.**	**0000h**
			15	Reserved	Reserved for extension of "other faults" in case of all the bits	0

			used up in this register.		
		14~7	Reserved		0
		6	PLD or Flash Initialization Fault	PLD, CPLD, or FPGA initialization fault. (FAWS_TYPE_A)	0
		5	Power Supply Fault	1: Power supply is out of range. (FAWS_TYPE_A)	0
		4~2	Reserved		000b
		1	CFP Checksum Fault	1: CFP Checksum failed. (FAWS_TYPE_A)	0
		0	Reserved		0

Figure 17: Module fault status

7.2.6. Corresponding MSA registers for A/D measurements

ACO mode:

B320 [2.0]	16	RO	15~0	Network Lane n TX Laser Bias Current monitor A/D value	16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent. Measured laser bias current in uA, a 16-bit unsigned integer with LSB = 2 uA, representing a total measurement range of 0 to 131.072 mA. Minimum accuracy shall be +/- 10% of the nominal value over temperature and voltage. This register is for CFP MSA modules.	0000h
B330 [2.0]	16	RO	15~0	Network Lane n TX Laser Output Power monitor A/D value	16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent. Measured TX laser output power in dBm, a signed 16-bit integer with LSB = 0.01 dBm. Accuracy must be better than +/- 2 dB over temperature and voltage range. Relative accuracy must be better than 1 dB.	0000h
B340 [2.0]	16	RO	15~0	Network Lane n TX Laser Temp Monitor A/D value	16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent. Internally measured temperature in degrees Celsius, a 16-bit signed integer with LSB = 1/256 of a degree Celsius, representing a total range from -128 to + 127 255/256 degC. MSA valid range is between –40 and +125C. Minimum accuracy is +/- 3 degC over temperature range.	0000h
B350 [2.0]	16	RO	15~0	Network Lane n RX Input Power monitor A/D value	16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent. Measured received input power in uW, a 16-bit unsigned integer with LSB = 0.1 uW, representing a power range from 0 to 6.5535 mW (-40 to +8.2 dBm). Value can represent either average received power or OMA depending upon how bit 3 of Register 8080h is set. Accuracy must be better than +/- 2dB over temperature and voltage. This accuracy shall be maintained for input power levels up to the lesser of maximum transmitted or maximum received optical power per the appropriate standard. It shall be maintained down to the minimum transmitted power minus	0000h

Figure 18: A/D value measurements (ACO)

Normal mode:

A2A0	16	RO	15~0	Network Lane n Laser Bias Current monitor A/D value	16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, ..., N-1. N_max = 16. Actual N is module dependent. Measured laser bias current in uA, a 16-bit unsigned integer with LSB = 2 uA, representing a total measurement range of 0 to 131.072 mA. If Ethernet Application Code (8003h) is "-Coherent", then LSB is changed to 100uA. (Range is expanded to 0 ~ 6553.5 mA). Minimum accuracy shall be +/- 10% of the nominal value over temperature and voltage.	0000h
A2B0	16	RO	15~0	Network Lane n Laser Output Power monitor A/D value	16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, ..., N-1. N_max = 16. Actual N is module dependent. Measured TX output power in uW, a 16-bit unsigned integer with LSB = 0.1 uW, representing a range of laser output power from 0 to 6.5535 mW (-40 to +8.2 dBm). Accuracy must be better than +/- 2 dB over temperature and voltage range. Relative accuracy must be better than 1 dB.	0000h
A2C0	16	RO	15~0	Network Lane n Laser Temp Monitor A/D value	16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, ..., N-1. N_max = 16. Actual N is module dependent. Internally measured temperature in degrees Celsius, a 16-bit signed integer with LSB = 1/256 of a degree Celsius, representing a total range from -128 to + 127 255/256 degC. MSA valid range is between –40 and +125C. Minimum accuracy is +/- 3 degC over temperature range.	0000h
A2D0	16	RO	15~0	Network Lane n Receiver Input Power monitor A/D value	16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, ..., N-1. N_max = 16. Actual N is module dependent. Measured received input power in uW, a 16-bit unsigned integer with LSB = 0.1 uW, representing a power range from 0 to 6.5535 mW (-40 to +8.2 dBm). Value can represent either average received power or OMA depending upon how bit 3 of Register 806Eh is set. Accuracy must be better than +/- 2dB over temperature and voltage. This accuracy shall be maintained for input power levels up to the lesser of maximum transmitted or maximum received optical power per the appropriate standard. It shall be maintained down to the minimum transmitted power minus cable plant loss per the appropriate standard. Relative accuracy shall be better than 1 dB over the received power range, temperature range, voltage range, and the life of the product.	0000h

Figure 19: A/D value measurements

7.3. Interrupt Masks tab

This tab will be updated in later releases. For this version of the GUI (V1.0.0), the channel monitor interrupt masks are disabled.

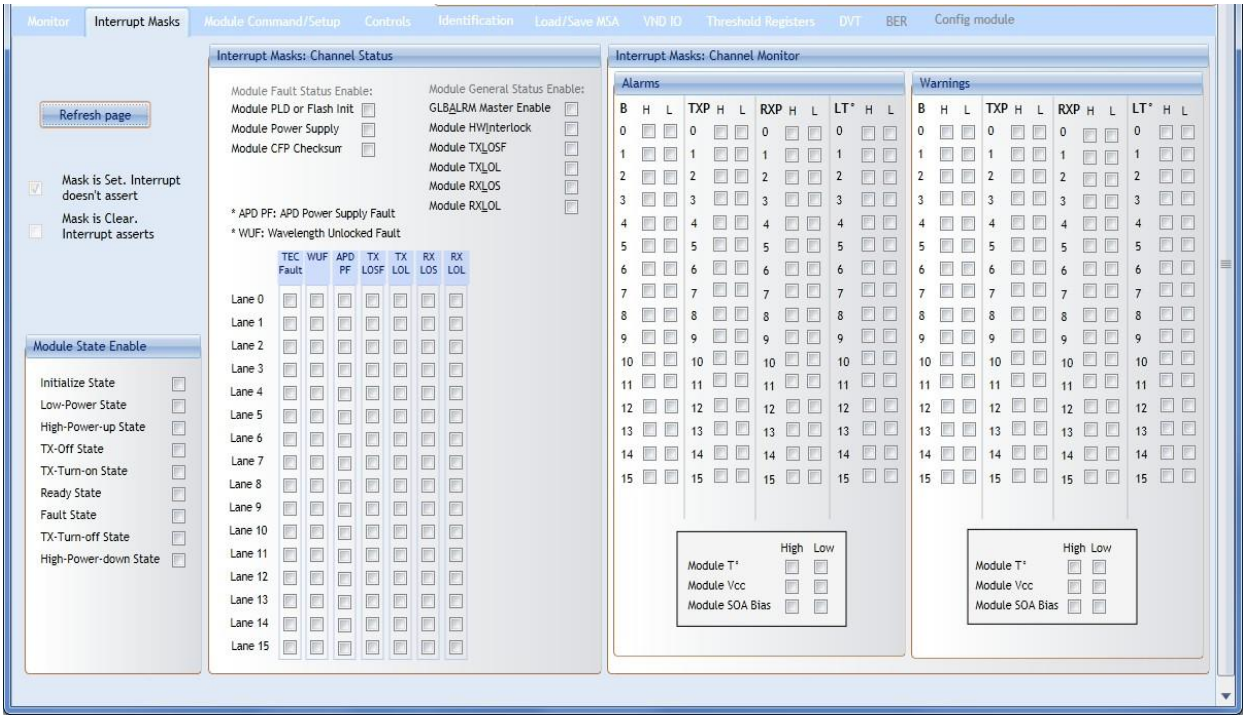


Figure 20: Interrupt Masks tab

7.3.1. Corresponding MSA registers for alarms and warning enable

ACO mode:

B1E0 [2.0]	16	RW		Network Lane n Alarm and Warning 1 Enable	16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent.	FFFF h
			15	Bias High Alarm Enable	0: Disable, 1: Enable.	1
			14	Bias High Warning Enable	0: Disable, 1: Enable.	1
			13	Bias Low Warning Enable	0: Disable, 1: Enable.	1
			12	Bias Low Alarm Enable	0: Disable, 1: Enable.	1
			11	TX Power High Alarm Enable	0: Disable, 1: Enable.	1
			10	TX Power High Warning Enable	0: Disable, 1: Enable.	1
			9	TX Power Low Warning Enable	0: Disable, 1: Enable.	1
			8	TX Power Low Alarm Enable	0: Disable, 1: Enable.	1
			7	Laser Temperature High Alarm Enable	0: Disable, 1: Enable.	1
			6	Laser Temperature High Warning Enable	0: Disable, 1: Enable.	1
			5	Laser Temperature Low Warning Enable	0: Disable, 1: Enable.	1
			4	Laser Temperature Low Alarm Enable	0: Disable, 1: Enable.	1
			3	RX Power High Alarm Enable	0: Disable, 1: Enable This comment applies to bits 2~0 as well.. The thresholds for the RX Power High/Low Alarm/Warning are determined by the RX Power Monitor Alarm/Warning Threshold Select in B015h.	1
			2	RX Power High Warning Enable	0: Disable, 1: Enable.	1
			1	RX Power Low Warning Enable	0: Disable, 1: Enable.	1
			0	RX Power Low Alarm Enable	0: Disable, 1: Enable.	1

Figure 21: Interrupt masks channel monitor (ACO)

Normal mode:

A240	16	RW		Network Lane n Alarm and Warning Enable	16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent.	FFFFh
			15	Bias High Alarm Enable	0: Disable, 1: Enable.	1
			14	Bias High Warning Enable	0: Disable, 1: Enable.	1
			13	Bias Low Warning Enable	0: Disable, 1: Enable.	1
			12	Bias Low Alarm Enable	0: Disable, 1: Enable.	1
			11	TX Power High Alarm Enable	0: Disable, 1: Enable.	1
			10	TX Power High Warning Enable	0: Disable, 1: Enable.	1
			9	TX Power Low Warning Enable	0: Disable, 1: Enable.	1
			8	TX Power Low Alarm Enable	0: Disable, 1: Enable.	1
			7	Laser Temperature High Alarm Enable	0: Disable, 1: Enable.	1
			6	Laser Temperature High Warning Enable	0: Disable, 1: Enable.	1
			5	Laser Temperature Low Warning Enable	0: Disable, 1: Enable.	1
			4	Laser Temperature Low Alarm Enable	0: Disable, 1: Enable.	1
			3	RX Power High Alarm Enable	0: Disable, 1: Enable.	1
			2	RX Power High Warning Enable	0: Disable, 1: Enable.	1
			1	RX Power Low Warning Enable	0: Disable, 1: Enable.	1
			0	RX Power Low Alarm Enable	0: Disable, 1: Enable.	1

Figure 22: Interrupt masks channel monitor

7.3.2. Corresponding MSA registers for fault and status enable

ACO mode:

B200 [2.0]	**16**			**Network Lane n Fault and Status Enable**	**16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent.**	**E0D Ch**
		RW	15	Lane TEC Fault Enable	0: Disable, 1: Enable.	1
		RW	14	Lane Wavelength Unlocked Fault Enable	0: Disable, 1: Enable.	1
		RW	13	Lane APD Power Supply Fault Enable	0: Disable, 1: Enable.	1
		RO	12~8	Reserved		0
		RW	7	Lane TX_LOSF Enable	0: Disable, 1: Enable.	1
		RW	6	Lane TX_LOL Enable	0: Disable, 1: Enable.	1
		RO	5	Reserved		0
		RW	4	Lane RX_LOS Enable	0: Disable, 1: Enable.	1
		RW	3	Lane RX_LOL Enable	0: Disable, 1: Enable.	1
		RW	2	Lane RX FIFO Status Enable	0: Disable, 1: Enable.	1
		RW	1	Lane RX TEC Fault Enable	0: Disable, 1: Enable.	1
		RO	0	Reserved		0

Figure 23: Interrupt masks Channel status (ACO)

Normal mode:

A250	**16**			**Network Lane n Fault and Status Enable**	**16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent.**	**E0DC h**
		RW	15	Lane TEC Fault Enable	0: Disable, 1: Enable.	1
		RW	14	Lane Wavelength Unlocked Fault Enable	0: Disable, 1: Enable.	1
		RW	13	Lane APD Power Supply Fault Enable	0: Disable, 1: Enable.	1
		RO	12~8	Reserved		0
		RW	7	Lane TX_LOSF Enable	0: Disable, 1: Enable.	1
		RW	6	Lane TX_LOL Enable	0: Disable, 1: Enable.	1
		RO	5	Reserved		0
		RW	4	Lane RX_LOS Enable	0: Disable, 1: Enable.	1
		RW	3	Lane RX_LOL Enable	0: Disable, 1: Enable.	1
		RW	2	Lane RX FIFO Status Enable	0: Disable, 1: Enable.	1
		RO	1~0	Reserved		0

Figure 24: Interrupt masks Channel status

7.3.3. Corresponding MSA registers for module fault status enable

ACO mode:

B02A [2.0]	**1**			**Module Fault Status Enable**	**These bits are AND'ed with corresponding bits in the Module Fault Latch register; the result is used to assert GLB_ALRM. Optional features that are not implemented shall have their Enable bit forced to '0'.**	**0062h**
		RO	15~7	Reserved		0
		RW	6	PLD or Flash Initialization Fault Enable	1: Enable.	1
		RW	5	Power Supply Fault Enable	1: Enable.	1
		RO	4~2	Reserved		000b
		RW	1	CFP Checksum Fault Enable	1: Enable.	1
		RO	0	Reserved		0

Figure 25: Module fault status enable (ACO)

Normal mode:

A02A	**1**			**Module Fault Status Enable**	**These bits are AND'ed with corresponding bits in the Module Fault Latch register; the result is used to assert GLB_ALRM. Optional features that are not implemented shall have their Enable bit forced to '0'.**	**0062h**
		RO	15~7	Reserved		0
		RW	6	PLD or Flash Initialization Fault Enable	1: Enable.	1
		RW	5	Power Supply Fault Enable	1: Enable.	1
		RO	4~2	Reserved		000b
		RW	1	CFP Checksum Fault Enable	1: Enable.	1
		RO	0	Reserved		0

Figure 26: Module fault status enable

7.3.4. Corresponding MSA registers for module general status enable

ACO mode:

B029 [2.0]	**1**			**Module General Status Enable**	**1: Enable signal to assert GLB_ALRM. Bits 14~0 are AND'ed with corresponding bits in the Module General Status Latch register; the result is used to assert GLB_ALRM. Bit 15 is the master enable of GLB_ALRM and it is AND'ed with the output of the "OR" gate output in Global Alarm Signal Aggregation, Figure 10.**	**A7F8h**
		RW	15	GLB_ALRM Master Enable	1: Enable.	1
		RO	14	Reserved		0
		RW	13	HW_Interlock	1: Enable. For non-pluggable modules (e.g. MSA-100GLH module), this bit is not read.	1
		RO	12~11	Reserved		0
		RW	10	Loss of REFCLK Input Enable	1: Enable.	1
		RW	9	TX_JITTER_PLL_LOL Enable	1: Enable.	1
		RW	8	TX_CMU_LOL Enable	1: Enable.	1
		RW	7	TX_LOSF Enable	1: Enable.	1
		RW	6	TX_HOST_LOL Enable	1: Enable.	1
		RW	5	RX_LOS Enable	1: Enable.	1
		RW	4	RX_NETWORK_LOL Enable	1: Enable.	1
		RW	3	Out of Alignment Enable	1. Enable.	1
		RW	2	Performance Monitor Interval Complete Enable	1. Enable.	1
		RO	1~0	Reserved		000b

Figure 27: Module general status enable (ACO)

A029	**1**			**Module General Status Enable**	**1: Enable signal to assert GLB_ALRM. Bits 14~0 are AND'ed with corresponding bits in the Module General Status Latch register; the result is used to assert GLB_ALRM. Bit 15 is the master enable of GLB_ALRM and it is AND'ed with the output of the "OR" gate output in Global Alarm Signal Aggregation, Figure 10.**	**A7F8h**
		RW	15	GLB_ALRM Master Enable	1: Enable.	1
		RO	14	Reserved		0
		RW	13	HW_Interlock	1: Enable.	1
		RO	12~11	Reserved		0
		RW	10	Loss of REFCLK Input Enable	1: Enable.	1
		RW	9	TX_JITTER_PLL_LOL Enable	1: Enable.	1
		RW	8	TX_CMU_LOL Enable	1: Enable.	1
		RW	7	TX_LOSF Enable	1: Enable.	1
		RW	6	TX_HOST_LOL Enable	1: Enable.	1
		RW	5	RX_LOS Enable	1: Enable.	1
		RW	4	RX_NETWORK_LOL Enable	1: Enable.	1
		RW	3	Out of Alignment Enable	1. Enable.	1
		RO	2~0	Reserved		000b

Figure 28: Module general status enable

7.3.5. Corresponding MSA registers for module state enable

ACO mode:

A028	**1**			**Module State Enable**	**GLB_ALRM Enable register for Module State change. One bit for each state.**	**006Ah**
		RO	15~9	Reserved		0
		RW	8	High-Power-down State Enable	1: Enable corresponding signal to assert GLB_ALRM.	0
		RW	7	TX-Turn-off State Enable	1: Enable corresponding signal to assert GLB_ALRM.	0
		RW	6	Fault State Enable	1: Enable corresponding signal to assert GLB_ALRM. (Init Value is 1 to allow GLB_ALRM in startup sequence.)	1
		RW	5	Ready State Enable	1: Enable corresponding signal to assert GLB_ALRM. (Init Value is 1 to allow GLB_ALRM in startup sequence.)	1
		RW	4	TX-Turn-on State Enable	1: Enable corresponding signal to assert GLB_ALRM.	0
		RW	3	TX-Off State Enable	1: Enable corresponding signal to assert GLB_ALRM. (Init Value is 1 to allow GLB_ALRM in startup sequence.)	1
		RW	2	High-Power-up State Enable	1: Enable corresponding signal to assert GLB_ALRM.	0
		RW	1	Low-Power State Enable	1: Enable corresponding signal to assert GLB_ALRM. (Init Value is 1 to allow GLB_ALRM in startup sequence)	1
		RO	0	Initialize State Enable	1: Enable corresponding signal to assert GLB_ALRM.	0

Figure 29: Module state enable (ACO)

B029 [2.0]	**1**			**Module General Status Enable**	**1: Enable signal to assert GLB_ALRM. Bits 14~0 are AND'ed with corresponding bits in the Module General Status Latch register; the result is used to assert GLB_ALRM. Bit 15 is the master enable of GLB_ALRM and it is AND'ed with the output of the "OR" gate output in Global Alarm Signal Aggregation, Figure 10.**	**A7F8h**
		RW	15	GLB_ALRM Master Enable	1: Enable.	1
		RO	14	Reserved		0
		RW	13	HW_Interlock	1: Enable. For non-pluggable modules (e.g. MSA-100GLH module), this bit is not read.	1
		RO	12~11	Reserved		0
		RW	10	Loss of REFCLK Input Enable	1: Enable.	1
		RW	9	TX_JITTER_PLL_LOL Enable	1: Enable.	1
		RW	8	TX_CMU_LOL Enable	1: Enable.	1
		RW	7	TX_LOSF Enable	1: Enable.	1
		RW	6	TX_HOST_LOL Enable	1: Enable.	1
		RW	5	RX_LOS Enable	1: Enable.	1
		RW	4	RX_NETWORK_LOL Enable	1: Enable.	1
		RW	3	Out of Alignment Enable	1. Enable.	1
		RW	2	Performance Monitor Interval Complete Enable	1. Enable.	1
		RO	1~0	Reserved		000b

Figure 30: Module state enable

7.3.6. Corresponding MSA registers for module alarm and warning enable

ACO mode:

B02B [2.0]	**1**			**Module Alarm and Warning 1 Enable**	**These bits are AND'ed with corresponding bits in the Module Alarm and Warning 1 Latch register; the result is used to assert GLB_ALRM. Optional features that are not implemented shall have their Enable bit forced to '0'.**	**0FFFh**
		RO	15~12	Reserved		0000b
		RW	11	Mod Temp Hi Alarm Enable	1: Enable.	1
			10	Mod Temp Hi Warn Enable	1: Enable.	1
			9	Mod Temp Low Warning Enable	1: Enable.	1
			8	Mod Temp Low Alarm Enable	1: Enable.	1
			7	Mod Vcc High Alarm Enable	1: Enable.	1
			6	Mod Vcc High Warning Enable	1: Enable.	1
			5	Mod Vcc Low Warning Enable	1: Enable.	1
			4	Mod Vcc Low Alarm Enable	1: Enable.	1
			3	Mod SOA Bias High Alarm Enable	1: Enable.	1
			2	Mod SOA Bias High Warning Enable	1: Enable.	1
			1	Mod SOA Bias Low Warning Enable	1: Enable.	1
			0	Mod SOA Bias Low Alarm Enable	1: Enable.	1

Figure 31: Module alarm and warning enable (ACO)

Normal mode:

A02B	1			Module Alarm and Warnings 1 Enable	These bits are AND'ed with corresponding bits in the Module Alarm and Warnings 1 Latch register; the result is used to assert GLB_ALRM. Optional features that are not implemented shall have their Enable bit forced to '0'.	0FFFh
		RO	15~12	Reserved		0000b
		RW	11	Mod Temp Hi Alarm Enable	1: Enable.	1
			10	Mod Temp Hi Warn Enable	1: Enable.	1
			9	Mod Temp Low Warning Enable	1: Enable.	1
			8	Mod Temp Low Alarm Enable	1: Enable.	1
			7	Mod Vcc High Alarm Enable	1: Enable.	1
			6	Mod Vcc High Warning Enable	1: Enable.	1
			5	Mod Vcc Low Warning Enable	1: Enable.	1
			4	Mod Vcc Low Alarm Enable	1: Enable.	1
			3	Mod SOA Bias High Alarm Enable	1: Enable.	1
			2	Mod SOA Bias High Warning Enable	1: Enable.	1
			1	Mod SOA Bias Low Warning Enable	1: Enable.	1
			0	Mod SOA Bias Low Alarm Enable	1: Enable.	1

Figure 32: Module alarm and warning enable

7.4. Controls tab

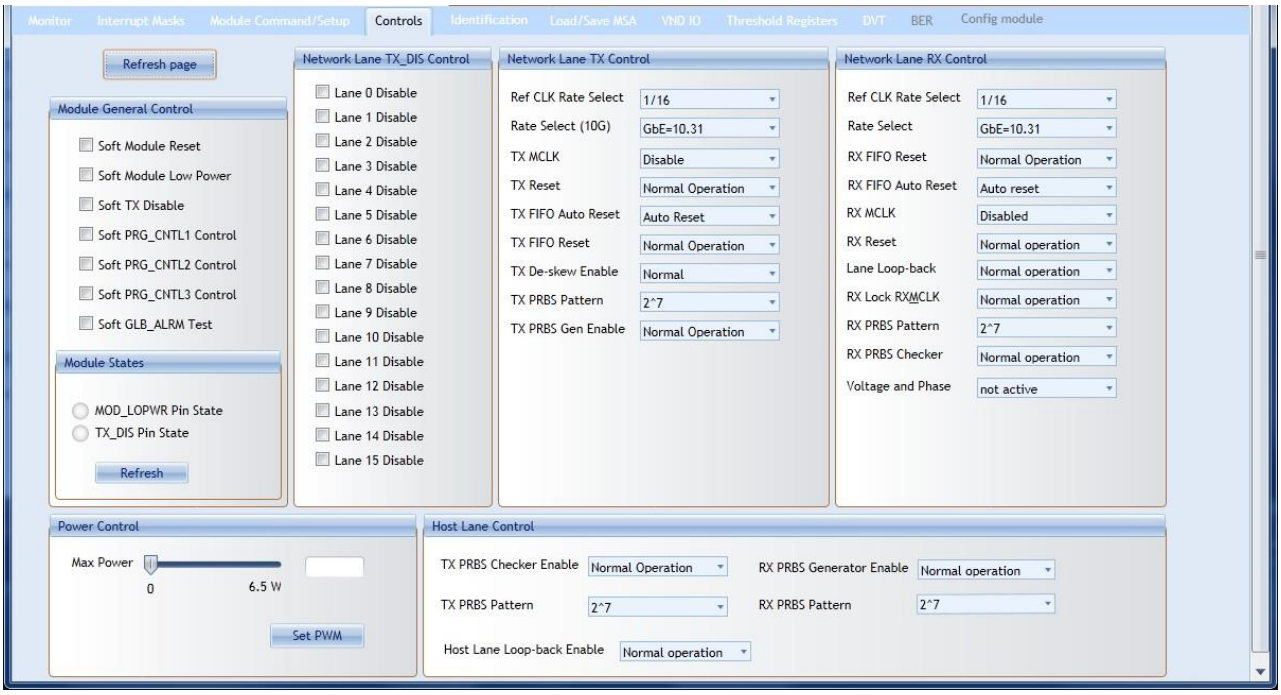


Figure 33: Controls tab

7.4.1. Power Control

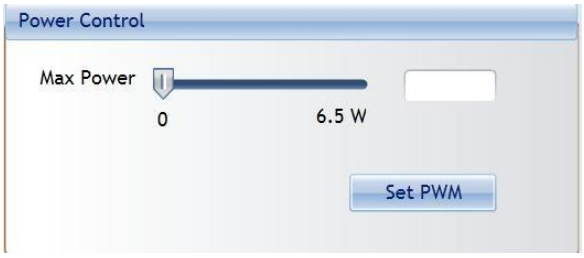


Figure 34: Power Control

The user can specify the maximum power consumed by the CFP8 module. He should adjust Max Power to the desired value, and then press Set PWM to set the maximum allowed values for each thermal spot. (Register **9401** is used).

7.4.2. Corresponding MSA registers for host Lane Control

ACO mode:

B014 [2.0]	**1**			**Host Lane Control**	**This control acts upon all the host lanes.**	**0000h**
		RO	15	Reserved		0
		RW	14	TX PRBS Checker Enable	0: Normal operation, 1: PRBS mode. (Optional)	0
		RW	13	TX PRBS Pattern 1	00:2^7, 01:2^15, 10:2^23, 11:2^31.	00b
		RW	12	TX PRBS Pattern 0		
		RO	11	Reserved		0
		RW	10	Host Lane Loop-back Enable	0: Normal operation, 1: Host lane loop-back. (Optional)	0
		RW	9 [2.4]	Automatic Host Lane Output Squelch on LOS (Optional)	0: Host Lane shall not squelch on RX_LOS. Host controls squelch using A040h 1: Host Lane shall squelch on RX_LOS (sync with A210h~A21Fh.4) per lane based.	0
		RW	8 [2.4]	Automatic Host Lane Output Squelch on LOL (Optional)	0: Host Lane shall not squelch on RX_LOL. Host controls squelch using A040h. 1: Host Lane shall squelch on RX_LOL (sync with A210h~A21Fh.3) per lane based.	0
		RW	7	RX PRBS Generator Enable	0: Normal operation, 1: PRBS mode. (Optional)	0
		RW	6	RX PRBS Pattern 1	00b: 2^7, 01b: 2^15, 10b: 2^23, 11b: 2^31.	00b
		RW	5	RX PRBS Pattern 0		
		RO	4~0	Reserved		0h

Figure 35: Host Lane Control (ACO)

Normal mode:

A014	**1**			**Host Lane Control**	**This control acts upon all the host lanes.**	**0000h**
		RO	15	Reserved		0
		RW	14	TX PRBS Checker Enable	0: Normal operation, 1: PRBS mode. (Optional)	0
		RW	13	TX PRBS Pattern 2	000b:2^7, 100b:2^23, 001b: 2^9, 101b: reserved, 010b:2^15, 110b:2^31, 011b: reserved, 111b: reserved.	000b
		RW	12	TX PRBS Pattern 1		
		RW	11	TX PRBS Pattern 0		
		RW	10	Host Lane Loop-back Enable	0: Normal operation, 1: Host lane loop-back. (Optional)	0
		RW	9	Automatic Host Lane Output Squelch on LOS (Optional)	0: Host Lane shall not squelch on RX_LOS. Host controls squelch using A040h 1: Host Lane shall squelch on RX_LOS (sync with A210h~A21Fh.4) per lane based.	0
		RW	8	Automatic Host Lane Output Squelch on LOL (Optional)	0: Host Lane shall Not squelch on RX_LOL. Host controls squelch using A040h. 1: Host Lane shall squelch on RX_LOL (sync with A210h~A21Fh.3) per lane based.	0
		RW	7	RX PRBS Generator Enable	0: Normal operation, 1: PRBS mode. (Optional)	0
		RW	6	RX PRBS Pattern 2	000b:2^7, 100b:2^23,	000b
		RW	5	RX PRBS Pattern 1	001b: 2^9, 101b: reserved, 010b:2^15, 110b:2^31, 011b: reserved, 111b: reserved.	
		RW	4	RX PRBS Pattern 0		
		RO	3~0	Reserved		0h

Figure 36: Host Lane Control

7.4.3. Corresponding MSA registers for individual network lane TX_DIS

ACO mode:

B013 [2.0]	**1**	**RW**		**Individual Network Lane TX_DIS Control**	**This register acts upon individual network lanes. Note that toggling individual network lane TX disable bit does not change module state.**	**0000h**
			15~0	Lane n Disable	Bits 15~0 disable Lanes 15~0 respectively. 0: Normal, 1: Disable.	0

Figure 37: Individual network lane TX_DIS (ACO)

Normal mode:

A013	**1**	**RW**		**Individual Network Lane TX_DIS Control**	**This register acts upon individual network lanes. Note that toggling individual network lane TX disable bit does not change module state.**	**0000h**
			15~0	Lane 15~0 Disable	Bits 15~0 disable Lanes 15~0 respectively. 0: Normal, 1: Disable.	0

Figure 38: Individual network lane TX_DIS

7.4.4. Corresponding MSA registers for module general control

ACO mode:

A010	**1**			**Module General Control**		**0000h**
		RW/SC/ LH	15	Soft Module Reset	Register bit for module reset function. Writing a 0 to this bit has no effect regardless it was 0 or 1 previously. 1: Module reset assert.	0
		RW	14	Soft Module Low Power	Register bit for module low power function. 1: Assert.	0
		RW	13	Soft TX Disable	Register bit for TX Disable function. 1: Assert.	0
		RW	12	Soft PRG_CNTL3 Control	Register bit for PRG_CNTL3 control function. 1: Assert.	0
		RW	11	Soft PRG_CNTL2 Control	Register bit for PRG_CNTL2 control function. 1: Assert.	0
		RW	10	Soft PRG_CNTL1 Control	Register bit for PRG_CNTL1 control function. 1: Assert.	0
		RW	9	Soft GLB_ALRM Test	Command bit for software forced test signal. When this bit is asserted it generates GLB_ALRM signal. 1: Assert.	0
		RO	8~6	Reserved		0
		RO	5	TX_DIS Pin State	Logical state of the TX_DIS pin. 1: Assert.	0
		RO	4	MOD_LOPWR Pin State	Logical state of the MOD_LOPWR pin. 1: Assert.	0

Figure 39: Module general control (ACO)

Normal mode:

B010 [2.0]	1			Module General Control		0000h
		RW/SC/LH	15	Soft Module Reset	Register bit for module reset function. Writing a 0 to this bit has no effect regardless it was 0 or 1 previously. 1: Module reset assert.	0
		RW	14	Soft Module Low Power	Register bit for module low power function. 1: Assert.	0
		RW	13	Soft TX Disable	Register bit for TX Disable function. 1: Assert.	0
		RW	12	Soft PRG_CNTL3 Control	Register bit for PRG_CNTL3 control function. 1: Assert.	0
		RW	11	Soft PRG_CNTL2 Control	Register bit for PRG_CNTL2 control function. 1: Assert.	0
		RW	10	Soft PRG_CNTL1 Control	Register bit for PRG_CNTL1 control function. 1: Assert.	0
		RW	9	Soft GLB_ALRM Test	Command bit for software forced test signal. When this bit is asserted it generates GLB_ALRM signal. 1: Assert.	0
		RW/SC	8	Processor Reset	Register bit for processor reset function. This bit is self-clearing. Register settings are not affected. This is a Non-Service Affecting reset. 1: Assert.	0
		RO	7~6	Reserved		0
		RO	5	TX_DIS Pin State	Logical state of the TX_DIS pin. 1: Assert.	0
		RO	4	MOD_LOPWR Pin State	Logical state of the MOD_LOPWR pin. 1: Assert.	0

Figure 40: Module general control

7.4.5. Corresponding MSA registers for network lane TX control

ACO mode:

B011 [2.0]	1			Network Lane TX Control	This control acts upon all the network lanes.	0200h
		RW	15 [2.4]	Automatic Network Lane TX Squelch Mode (Optional)	0: Network Lane shall squelch TX Average power on TX_LOL (sync with B1A0h~B1AFh.6) per lane base. 1: Network Lane shall squelch TX OMA power on TX_LOL (sync with B1A0h~B1AFh.6) per lane base.	0
		RW	14	TX PRBS Generator Enable	0: Normal operation, 1: PRBS mode. (Optional)	0
		RW	13~12	TX PRBS Pattern	00b:2^7, 01b:2^15, 10b:2^23, 11b:2^31.	00b
		RW	11	TX De-skew Enable	0:Normal, 1:Disable	0
		RW	10	TX FIFO Reset	This bit affects both host and network side TX FIFOs. 0: Normal operation, 1: Reset (Optional).	0
		RW	9	TX FIFO Auto Reset	This bit affects both host and network side TX FIFOs. 0: Not Auto Reset, 1: Auto Reset. (Optional).	1
		RW	8	TX Reset	0: Normal operation, 1: Reset. Definition and implementation is vendor specific.	0
		RW [2.2]	7~5	TX MCLK Control	3-bit field coding the MCLK rate control.	000b
		RW	4 [2.4]	Automatic Network Lane TX Squelch Control (Optional)	0: Network lane automatic control on TX_LOL is off. Host controls each lane output squelch using A041h. 1: Network lane automatic control on TX_LOL is on per lane base.	0
		RW	3~1	TX Rate Select (10G lane rate)	000b: GbE=10.31, 001b: SDH=9.95, 010b: OTU3=10.7, 011b: OTU4=11.2, 100b: OTU3e1=11.14, 101b: OTU3e2=11.15, 110b~111b: Reserved.	000b
		RW	0	TX Reference CLK Rate Select	0: 1/16, 1: 1/64.	0b

Code	Description	CFP	CFP2/4
000b	Function disabled		
001b	Of network lane rate	Reserved	1/32
010b	Of network lane rate	1/8	1/8
011b	Of host lane rate	Reserved	Reserved
100b	Of network lane rate	1/64	Reserved
101b	Of host lane rate	1/64	1/160
110b	Of network lane rate	1/16	Reserved
111b	Of host lane rate	1/16	1/40

Figure 41: Network lane TX control (ACO)

Normal mode:

A011	**1**			**Network Lane TX Control**	**This control acts upon all the network lanes.**	**0200h**
		RW	15 [2.4]	Automatic Network Lane TX Squelch Mode (Optional)	0: Network Lane shall squelch TX Average power on TX_LOL (sync with A210h~A21Fh.6) per lane base. 1: Network Lane shall squelch TX OMA power on TX_LOL (sync with A210h~A21Fh.6) per lane base.	0
		RW	14	TX PRBS Generator Enable	0: Normal operation, 1: PRBS mode. (Optional)	0
		RW	13~12	TX PRBS Pattern	Standard Modes (A015h.15 = 0) 00b:2^7, 01b:2^15, 10b:2^23, 11b:2^31, Extended Modes (A015h.15 = 1) 00b: 2^9, 01b: Reserved, 10b: Reserved, 11b: Reserved.	00b
		RW	11	TX De-skew Enable	0:Normal, 1:Disable	0
		RW	10	TX FIFO Reset	This bit affects both host and network side TX FIFOs. 0: Normal operation, 1: Reset (Optional).	0
		RW	9	TX FIFO Auto Reset	This bit affects both host and network side TX FIFOs. 0: Not Auto Reset, 1: Auto Reset. (Optional).	1
		RW	8	TX Reset	0: Normal operation, 1: Reset. Definition and implementation are vendor specific.	0
		RW [2.2]	7~5	TX MCLK Control	A 3-bit field coding the MCLK rate control.	000b

Code	Source Lane	CFP or CFP2 10x10 mode*	CFP2 4x25 mode* and CFP4*
000b	Function disabled		
001b	Of network lane rate	Reserved	1/32
010b	Of network lane rate	1/8	1/8
011b	Of host lane rate	Reserved	Reserved
100b	Of network lane rate	1/64	Reserved
101b	Of host lane rate	1/64	1/160
110b	Of network lane rate	1/16	Reserved
111b	Of host lane rate	1/16	1/40

		RW	4 [2.4]	Automatic Network Lane TX Squelch Control (Optional)	0: Network lane automatic control on TX_LOL is off. Host controls each lane TX squelch using A041h. 1: Network lane automatic control on TX_LOL is on per lane base.	0
		RW	3~1	TX Rate Select (Host Side)	A 3-bit field codes RX rate select implemented for a module. The selected rate is module ID and number of host lane dependent. Registers 8000h and 8009h shall be referenced to determine what signal type at what rate is supported.	000b or 110b

Code	CFP or CFP2 10x10 mode*	CFP2 4x25 mode*	CFP4*
	Signal Type and Rate Selected		
000b	GbE 10.31	GbE 25.8	GbE 25.8

					001b	SDH 9.95	Reserved	Reserved	
					010b	OTU3 10.7	Reserved	Reserved	
					011b	OTU4 11.2	OTU4 28	OTU4 28	
					100b	OTU3e1 11.14	Reserved	Reserved	
					101b	OTU3e2 11.15	Reserved	Reserved	
					110b	Reserved	Reserved	Reserved	
					111b	Reserved	Reserved	Reserved	
					* See 8000h for module ID and 8009h for Number of Host Lanes				
		RW	0	TX Reference CLK Rate Select	A 1-bit field codes TX Reference CLK rate select implemented for a module. The selected rate is module ID and number of host lane dependent. Registers 8000h and 8009h shall be referenced to determine what signal type at what rate is supported.				1b
					Code	CFP or CFP2 10x10 mode*	CFP2 4x25 mode*	CFP4*	
						CLK Divider			
					0b	1/16	1/40	1/40	
					1b	1/64	1/160	1/160	
					* See 8000h for module ID and 8009h for Number of Host Lanes				

Figure 42: Network lane TX control

7.4.6. Corresponding MSA registers for network lane RX control

ACO mode:

B012 [2.0]	**1**			**Network Lane RX Control**	**This control acts upon all the network lanes.**				**0200h**
		RW	15	Active Decision Voltage and Phase function	This bit activates the active decision voltage and phase function in the module. 0: not active, 1: active. (Optional)				0b
		RW	14	RX PRBS Checker Enable	0: Normal operation, 1: PRBS mode. (Optional)				0b
		RW	13~12	RX PRBS Pattern	00b: 2^7, 01b: 2^15, 10b: 2^23, 11b: 2^31.				00b
		RW	11	RX Lock RX_MCLK to Reference CLK	0: Normal operation, 1: Lock RX_MCLK to REFCLK.				0b
		RW	10	Network Lane Loop-back	0: Normal operation, 1: Network lane loop-back. (Optional)				0b
		RW	9	RX FIFO Auto Reset	0: Not auto reset, 1: Auto reset. (Optional).				1b
		RW	8	RX Reset	0: Normal operation, 1: Reset. Definition and implementation are vendor specific.				0b
		RW [2.2]	7~5	RX MCLK Control (optional)	3-bit field coding the MCLK rate control.				000b
					Code	**Description**	**CFP**	**CFP2/4**	
					000b	Function disabled			
					001b	Of network lane rate	Reserved	1/32	
					010b	Of network lane rate	1/8	1/8	
					011b	Of host lane rate	Reserved	Reserved	
					100b	Of network lane rate	1/64	Reserved	
					101b	Of host lane rate	1/64	1/160	
					110b	Of network lane rate	1/16	Reserved	
					111b	Of host lane rate	1/16	1/40	
		RW	4	RX FIFO Reset	0: Normal, 1: Reset. (Optional).				0b
		RW	3~1	RX Rate Select	000b: GbE=10.31, 001b:SDH=9.95, 010b:OTU3=10.7, 011b:OTU4=11.2, 100b:OTU3e1=11.14, 101b OTU3e2=11.15, 110b~111b: Reserved.				000b
		RW	0	RX Reference CLK Rate Select	0: 1/16, 1: 1/64.				1b

Figure 43: Network lane RX control (ACO)

Normal mode:

A012	**1**			**Network Lane RX Control**	**This control acts upon all the network lanes.**	**0200h**
		RW	15	Active Decision Voltage and Phase function	This bit activates the active decision voltage and phase function in the module. 0: not active, 1: active. (Optional)	0b
		RW	14	RX PRBS Checker Enable	0: Normal operation, 1: PRBS mode. (Optional)	0b
		RW	13~12	RX PRBS Pattern	Standard Modes (A015.14 = 0): 00b:2^7, 01b:2^15, 10b:2^23, 11b:2^31, Extended Modes (A015.14 = 1): 00b: 2^9, 01b: Reserved, 10b: Reserved, 11b: Reserved.	00b
		RW	11	RX Lock RX_MCLK to Reference CLK	0: Normal operation, 1: Lock RX_MCLK to REFCLK.	0b
		RW	10	Network Lane Loop-back	0: Normal operation, 1: Network lane loop-back. (Optional)	0b
		RW	9	RX FIFO Auto Reset	0: Not auto reset, 1: Auto reset. (Optional).	1b
		RW	8	RX Reset	0: Normal operation, 1: Reset. Definition and implementation are vendor specific.	0b
		RW [2.2]	7~5	RX MCLK Control (optional)	3-bit field coding the MCLK rate control.	000b
		RW	4	RX FIFO Reset	0: Normal, 1: Reset. (Optional).	0b
		RW	3~1	RX Rate Select (Host Side)	A 3-bit field codes RX rate select implemented for a module. The selected rate is module ID and number of host lane dependent. Registers 8000h and 8009h shall be referenced to determine what signal type at what rate is supported.	000b
		RW	0	RX Reference CLK Rate Select	A 1-bit field codes RX Reference CLK rate select implemented for a module. The selected rate is module ID and number of host lane dependent. Registers 8000h and 8009h shall be referenced to determine what signal type at what rate is supported.	1b

Code	Description	CFP or CFP2 10x10 mode	CFP2 4x25 mode or CFP4
000b	Function disabled		
001b	Of network lane rate	Reserved	1/32
010b	Of network lane rate	1/8	1/8
011b	Of host lane rate	Reserved	Reserved
100b	Of network lane rate	1/64	Reserved
101b	Of host lane rate	1/64	1/160
110b	Of network lane rate	1/16	Reserved
111b	Of host lane rate	1/16	1/40

Code	CFP or CFP2 10x10 mode*	CFP2 4x25 mode*	CFP4*
	Signal Type and Rate Selected		
000b	GbE 10.31	GbE 25.8	GbE 25.8
001b	SDH 9.95	Reserved	Reserved
010b	OTU3 10.7	Reserved	Reserved
011b	OTU4 11.2	OTU4 28	OTU4 28
100b	OTU3e1 11.14	Reserved	Reserved
101b	OTU3e2 11.15	Reserved	Reserved
110b	Reserved	Reserved	Reserved
111b	Reserved	Reserved	Reserved

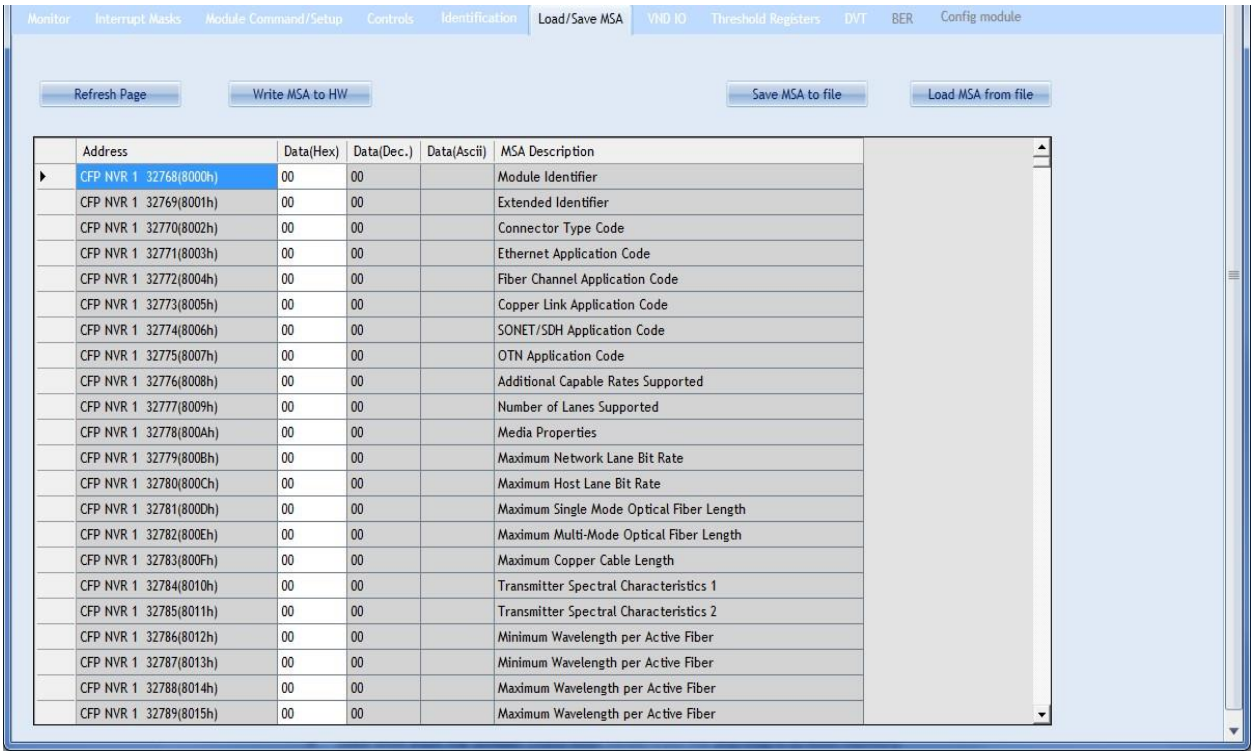
* See 8000h for module ID and 8009h for Number of Host Lanes

Code	CFP or CFP2 10x10 mode*	CFP2 4x25 mode*	CFP4*
	CLK Divider		
0b	1/16	1/40	1/40
1b	1/64	1/160	1/160

* See 8000h for module ID and 8009h for Number of Host Lanes

Figure 44: Network lane RX control

7.5. Load/Save MSA tab



Address	Data(Hex)	Data(Dec.)	Data(Ascii)	MSA Description
CFP NVR 1 32768(8000h)	00	00		Module Identifier
CFP NVR 1 32769(8001h)	00	00		Extended Identifier
CFP NVR 1 32770(8002h)	00	00		Connector Type Code
CFP NVR 1 32771(8003h)	00	00		Ethernet Application Code
CFP NVR 1 32772(8004h)	00	00		Fiber Channel Application Code
CFP NVR 1 32773(8005h)	00	00		Copper Link Application Code
CFP NVR 1 32774(8006h)	00	00		SONET/SDH Application Code
CFP NVR 1 32775(8007h)	00	00		OTN Application Code
CFP NVR 1 32776(8008h)	00	00		Additional Capable Rates Supported
CFP NVR 1 32777(8009h)	00	00		Number of Lanes Supported
CFP NVR 1 32778(800Ah)	00	00		Media Properties
CFP NVR 1 32779(800Bh)	00	00		Maximum Network Lane Bit Rate
CFP NVR 1 32780(800Ch)	00	00		Maximum Host Lane Bit Rate
CFP NVR 1 32781(800Dh)	00	00		Maximum Single Mode Optical Fiber Length
CFP NVR 1 32782(800Eh)	00	00		Maximum Multi-Mode Optical Fiber Length
CFP NVR 1 32783(800Fh)	00	00		Maximum Copper Cable Length
CFP NVR 1 32784(8010h)	00	00		Transmitter Spectral Characteristics 1
CFP NVR 1 32785(8011h)	00	00		Transmitter Spectral Characteristics 2
CFP NVR 1 32786(8012h)	00	00		Minimum Wavelength per Active Fiber
CFP NVR 1 32787(8013h)	00	00		Minimum Wavelength per Active Fiber
CFP NVR 1 32788(8014h)	00	00		Maximum Wavelength per Active Fiber
CFP NVR 1 32789(8015h)	00	00		Maximum Wavelength per Active Fiber

Figure 45: Load/Save MSA tab

This screen allows user to Load or Save his custom CFP8/CFP8-ACO configuration.

Once data is gathered, it will be displayed in a grid showing: register address, hex value, ASCII value, register description.

- **Refresh Page button:** Read CFP MSA Registers, and refresh values.
- **Write MSA to HW button:** Write the current MSA configuration to CFP8 module.
- **Save MSA to file button:** saves the current MSA memory to a file using CSV (comma separated values) format.
- **Load MSA from file button:** Loads MSA values from file and map it to MSA memory.

Note that the user can choose from the drop down list whether to read/write:

- ✓ Volatile registers
- ✓ Non volatile registers
- ✓ All MSA registers without

P.S: These registers exclude the reserved addresses.

7.6. DVT tab

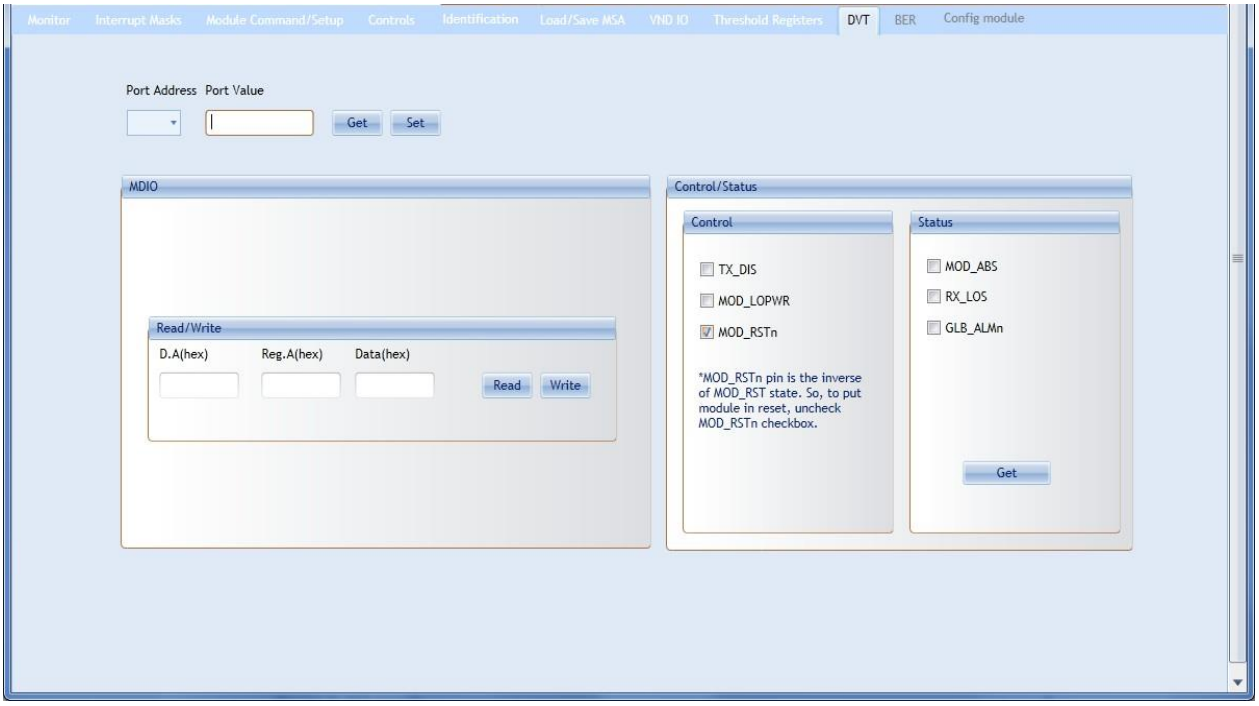


Figure 46: DVT tab

This tab allows the user to read/write MDIO registers directly from ML4057 micro, to control HW signals (TX_DIS, MOD_LOPWR, MOD_RSTn) and to get module status pins values (MOD_ABS, RX_LOS, GLB_ALMn).

D.A(hex): Device Address, in general set this value to 1.

Reg.A(hex): Register Address to read from or to write to.

Data(hex): Data read from the Reg.A or Data to be written to Reg.A.

8. API

An API file containing all the ML4057/ML4057-ACO functions can be provided; these functions allow access to the alarm and control signals as well as to the MDIO Master commands. Hence, users can implement these functions according to their own requests and using the platform that responds to their requirements.

Revision History

Revision	Description	Date
0.1	▪ Preliminary revision	13/10/2016

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